

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1                   1. (currently amended): A device for the emulation of designs for integrated  
2   circuits, comprising:  
3                    having a receiving device (1, 2, 3, 4, 5, 6) configured for receiving multiple  
4   programmable logic circuits having terminal contacts; (11, 12, 13; 21, 22, 23), particularly  
5   FPGAs, and  
6                    an electrical connection structure (14; 24), which has bus lines (111, 112, 121,  
7   122, 131, 132; 211, 212, 221, 222, 231, 232), each of which includes multiple channels (1...k),  
8   wherein  
9                    characterized in that,  
10                   [[ -     ]] each programmable logic circuit (11, 12, 13; 21, 22, 23) of the multiple  
11   programmable logic circuits when connected with the receiving device is connected to at least  
12   one bus line of the bus lines (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) and  
13                   [[ -     ]] wherein the electrical connection structure (14; 24) is implemented  
14   configured so it may be that the multiple programmable logic circuits are independently  
15   interconnectable with one another flexibly interconnected,  
16                   [[ -     ]] wherein in that the assignment of at least a part of the terminal contacts  
17   of any programmable logic circuit (11, 12, 13; 21, 22, 23) is independently assignable freely  
18   programmable and  
19                   [[ -     ]] wherein in that at least a part of the bus lines (111, 112, 121, 122, 131,  
20   132; 211, 212, 221, 222, 231, 232) connected to the programmable logic circuits (11, 12, 13; 21,  
21   22, 23) are alternately electrically connectable to one another using a switch wherein in such a  
22   way that at least one channel (1...k) of a bus line (111, 112, 121, 122, 131, 132; 211, 212, 221,

23 ~~222, 231, 232~~) is electrically connectable to a channel (1...k) of at least one other bus line (~~111,~~  
24 ~~112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232~~) using a the switch (~~S<sub>1</sub>...S<sub>k</sub>~~).

1                   2. (currently amended): The device according to Claim 1,  
2                   ~~characterized in that~~ wherein the multiple channels (1...k) of a bus line (~~111, 112,~~  
3 ~~121, 122, 131, 132; 211, 212, 221, 222, 231, 232~~) are alternately electrically connectable to  
4 multiple channels (1...k) of another bus line (~~111, 112, 121, 122, 131, 132; 211, 212, 221, 222,~~  
5 ~~231, 232~~), each channel (1...k) of the one bus line (~~111, 112, 121, 122, 131, 132; 211, 212, 221,~~  
6 ~~222, 231, 232~~) being electrically connectable to the ~~assigned~~ channel (1...k) of the other bus line  
7 (~~111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232~~), the individual channels of the  
8 multiple channels (1...k) being connectable independently of one another.

1                   3. (currently amended): The device according to Claim 1,  
2                   ~~characterized in that~~ comprising connection bus lines (~~15, 16, 17; 25, 26, 27~~) are  
3 ~~provided~~ between at least a part of the programmable logic circuits (~~11, 12, 13; 21, 22, 23~~) for  
4 direct connection of at least a part of the programmable ~~the corresponding~~ logic circuits (~~11, 12,~~  
5 ~~13; 21, 22, 23~~).

1                   4. (currently amended): The device according to Claim 1, being one of multiple  
2 receiving devices and ~~characterized in that~~ wherein the multiple receiving devices (~~1, 2; 3, 4; 5, 6~~)  
3 are connectable to one another via connection devices (~~7A, 7B, 7C; 9A, 9B~~), the connection  
4 devices (~~7A, 7B, 7C; 9A, 9B~~) having switchable bus lines.

1                   5. (currently amended): The device according to Claim 4,  
2                   ~~characterized in that~~ further comprising main connection devices (~~7A, 7B, 7C~~) ~~are~~  
3 ~~provided~~, each of which connects two receiving devices (~~1, 2; 3, 4; 5, 6~~) to one another, the main  
4 connection devices (~~7A, 7B, 7C~~) having main connection device bus lines (~~711, 712, 721, 722,~~  
5 ~~731, 732~~), which connect the ~~particular~~ bus lines (~~111, 112, 121, 122, 131, 132; 211, 212, 221,~~  
6 ~~222, 231, 232~~) of the two receiving devices (~~1, 2~~) assigned to one another to one another and the

7 main connection device bus lines (711, 712, 721, 722, 731, 732) of a ~~main connection device~~  
8 (7A, 7B, 7C) being alternately electrically connectable to one another in such a way that at least  
9 one channel (1...k) of a main connection device bus line (711, 712, 721, 722, 731, 732) is  
10 electrically connectable to the channel (1...k) of at least one other main connection device bus  
11 line (711, 712, 721, 722, 731, 732).

1 6. (currently amended): The device according to Claim 5,  
2 characterized in that further comprising group connection devices (9A, 9B) are  
3 provided, each of which connects two receiving device pairs, including two receiving devices (1,  
4 2; 3, 4; 5, 6), connected to one another using a the main connection device (7A, 7B, 7C), to one  
5 another and a group connection device (9A, 9B) having group connection device bus lines (911,  
6 912, 913, 914, 915, 916), which are connected to the bus lines of the ~~particular~~ receiving device  
7 pair (1, 2; 3, 4; 5, 6), and the group connection device bus lines (911, 912, 913, 914, 915, 916) of  
8 the ~~group connection devices~~ (9A, 9B) each being switchable in such a way that each channel  
9 (1...k) of each group connection device bus line (911, 912, 913, 914, 915, 916) of the group  
10 connection device (9A, 9B) is assigned one of a plurality of switches a switch (S<sub>1</sub>...S<sub>k</sub>) and  
11 wherein each switch of the plurality of the switches is configured to be the particular switches  
12 ~~may be~~ switched on and off independently of the other switches of the plurality of switches ~~one~~  
13 ~~another~~.

1 7. (currently amended): The device according to Claim 4 6,  
2 characterized in that wherein the receiving devices (1, 2, 3, 4, 5, 6), the main  
3 connection devices (7A, 7B, 7C), and the group connection devices (9A, 9B) have circuit boards  
4 (10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B), which are provided on their upper side and  
5 on their lower side with plug connector arrangements (V<sub>0</sub>, V<sub>1</sub>) which include multiple plug  
6 connectors situated in the same position on the ~~particular~~ circuit boards (10, 20, 30, 40, 50, 60;  
7 70A, 70B, 70C; 90A, 90B) and the outward-leading bus lines of the ~~particular~~ circuit boards (10,  
8 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B) are electrically connected to both upper and

9 corresponding lower plug connectors of the ~~particular~~ plug connector arrangement ( $V_O$ ,  $V_U$ ) in  
10 the same way.

1 8. (currently amended): The device according to Claim 7,  
2 ~~characterized in that~~ wherein the circuit boards (~~10, 20, 30, 40, 50, 60; 70A, 70B,~~  
3 ~~70C; 90A, 90B~~) are positioned one over another and are mechanically and electrically connected  
4 to one another using the plug connector arrangements ( $V_O$ ,  $V_U$ ),  
5 and wherein two circuit boards (~~10, 20, 30, 40, 50, 60~~) at a time of the receiving  
6 devices (~~1, 2; 3, 4; 5, 6~~) being are connected ~~like a sandwich~~ into a receiving device pair using a  
7 circuit board (~~70A, 70B, 70C~~) of a main connection device (~~7A, 7B, 7C~~) positioned between the  
8 two circuit boards of the receiving devices, to form a receiving-device-main-connection-device  
9 circuit board stack ~~them~~  
10 and wherein the receiving device pair is one of several receiving device pairs and  
11 wherein the receiving device pairs ~~being are~~ connected to one another using the circuit boards  
12 (~~90A, 90B~~) of the group connection devices (~~9A, 9B~~).

1 9. (currently amended): The device according to Claim 7 8,  
2 ~~characterized in that~~ wherein a spacing ( $L$ ) is provided between some of the plug  
3 connectors of the ~~particular~~ plug connector arrangements ( $V_O$ ,  $V_U$ ), the spacing being  
4 dimensioned to allow ~~which allows~~ cool air to flow through the circuit board stack ~~sandwich~~  
5 between the plug connectors.

10. (canceled)

1 11. (new) The device of Claim 1, wherein the multiple programmable logic  
2 circuits comprise FPGAs.